Innovation in IoT

Chili2S Module Datasheet

Rev. 0.5, September 2019

GENERAL DESCRIPTION

The Chili2S module is a fully-featured Thread-certified wireless module solution for IEEE 802.15.4 communications in the 2.4GHz band. It pairs the Cascoda CA-8211 SMARTRange™ transceiver modem with the Nuvoton M2351 Cortex®-M23 TrustZone® microcontroller.

With industry leading power consumption and sensitivity performance, it delivers unparalleled range without external amplifier components, thus providing whole-house connectivity in any market on the planet.

FEATURES

- SMARTRange™ CA-8211 IEEE 802.15.4 modem
  - Thread-certified component for every role
  - Industry-leading receive sensitivity of -105dBm
  - Programmable transmit power of -3dBm to +9dBm
  - Industry-leading link budget of 114dB
  - Integrated MAC low-power co-processor
- NuMicro® M2351 TrustZone® MCU
  - Arm® Cortex®-M23 Architecture
  - Highly robust security for IoT applications
  - 512 KB dual-bank application ROM (APROM) for Over-The-Air (OTA) upgrade
  - 96 KB on-chip SRAM
  - Communication interfaces (UART, I2C, SPI, USB)
  - Analog Interfaces (ADC, DAC, Comp)
  - Smart Card (ISO 7816) and SD Card Interfaces
- World-class energy consumption
  - World's best receiver efficiency
    14mA (42mW) at -105dBm sensitivity (0.0316nW)
    Figure of Merit (FoM) 0.75 $(mW*nW)^{-1}$
  - 19mA at +9dBm transmit power
  - 3µA sleep mode
- Industrial temperature range: -40°C to +85°C
- Wide supply voltage range: 2.1V to 3.6V
- Chip antenna and all other RF components integrated on module
- 16 MHz crystal for system clock and 32.768 kHz crystal for low-power RTC functionality
- Module size: 27.00 x 21.05 mm

DEVELOPMENT TOOLS

- Certified Thread stack based on OpenThread
- Optimised interface for the M2351 MCU and the CA8211 hardware MAC
- Module can be detached node running the network stack and application or coprocessor for hosts running Linux within a Thread mesh network
- Cascoda SDK, making full use of CMake as a build system
- Code available open-source on GitHub

BENEFITS

Equipment cost: Increased range removes the need for external power amplifiers, thereby reducing component BOM.

Installation cost: Greater datalink reliability lessens the need for skilled installers, and the consumer can self-install.

Maintenance cost: Lower power consumption means that batteries last longer, thereby minimising maintenance cost.

Development time: Use of pre-certified module minimises product development time.

APPLICATIONS

- Home and building automation
- Consumer electronics
- Lighting systems
- Heating, ventilation & air-conditioning systems (HVAC)
- Smart grid (AMI/AMR)
- Asset tracking (active RFID)
- Industrial control and monitoring
- Assisted living & telecare

Table of Contents

1 Overview

The Chili2S module is a highly-integrated module for developing Thread® / IEEE 802.15.4 low-power wireless personal area network (WPAN) applications. It combines the Nuvoton M2351 Cortex®-M23 TrustZone® microcontroller with the Cascoda CA-8211 Thread® certified 2.4 GHz IEEE 802.15.4 transceiver modem. The main features of the Chili2S module are:

- Nuvoton M2351 Arm® Cortex®-M23 TrustZone® MCU
  - Arm® TrustZone® technology
  - 512k bytes of Flash Application ROM (APROM) memory, dual bank for Over-The-Air (OTA) upgrade
  - 96k bytes of SRAM
  - Up to 64MHz core frequency
- Cascoda SMARTRange™ CA-8211 IEEE 802.15.4 2.4 GHz transceiver modem
  - Thread® certified component for every role
  - Industry-leading link budget of 114 dB
  - -105 dBm receiver sensitivity
  - Up to 9dBm transmit power
  - 19mA transmit current consumption at 9dBm
  - 14mA receive current consumption
  - 200nA low-power mode
- Module sleep current as low as 3uA
- 16MHz crystal oscillator supplying the system clock for both radio and MCU
- 32.768 kHz crystal oscillator for low-power RTC functionality
- Pin access via edge pads to
  - Up to 14 digital GPIOs with mappable Multi-Function Pin (MFP) functionality
  - Communication interfaces (UART, I2C, SPI, USB)
  - Analog Interfaces (ADC, DAC, comparator)
- SMD chip antenna

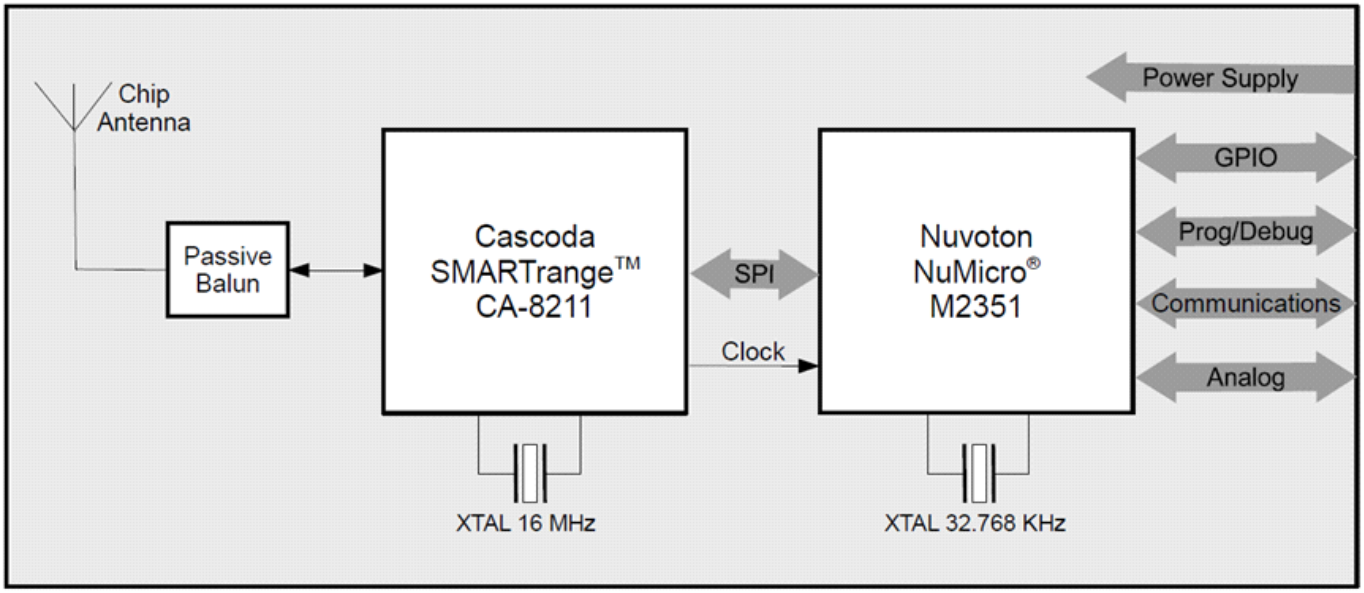

Figure 1.1: Chili2S Block Diagram

2 Hardware Description

2.1 Module Pin Configuration

The following figure shows the front view of the Chili2S module. The edge pads (Pin1 to Pin42) for solder-down are on 1.27mm pitch.

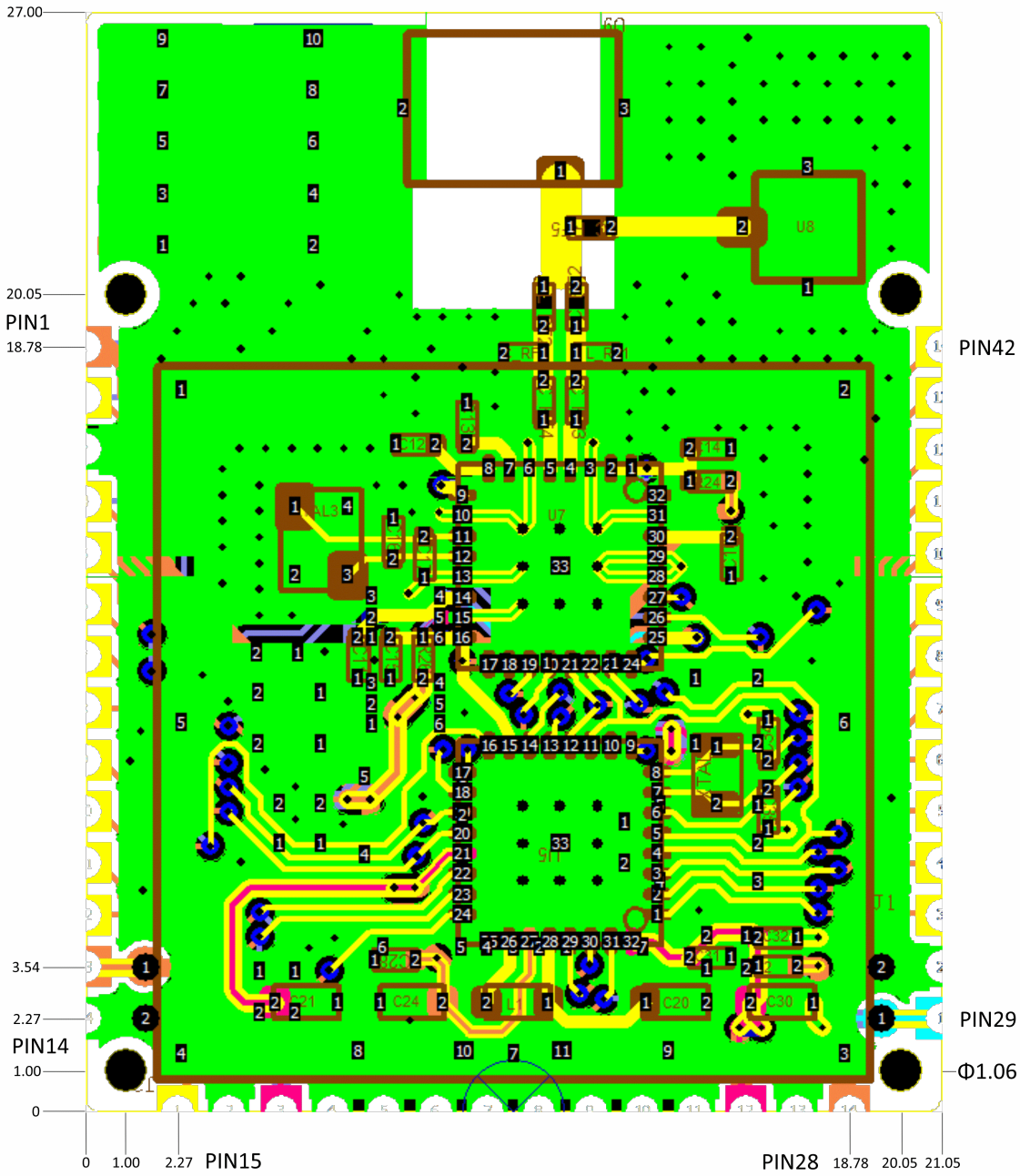

Figure 2.1: Chili2S Module Front View (Unit:mm)

2.2 Recommended Footprint

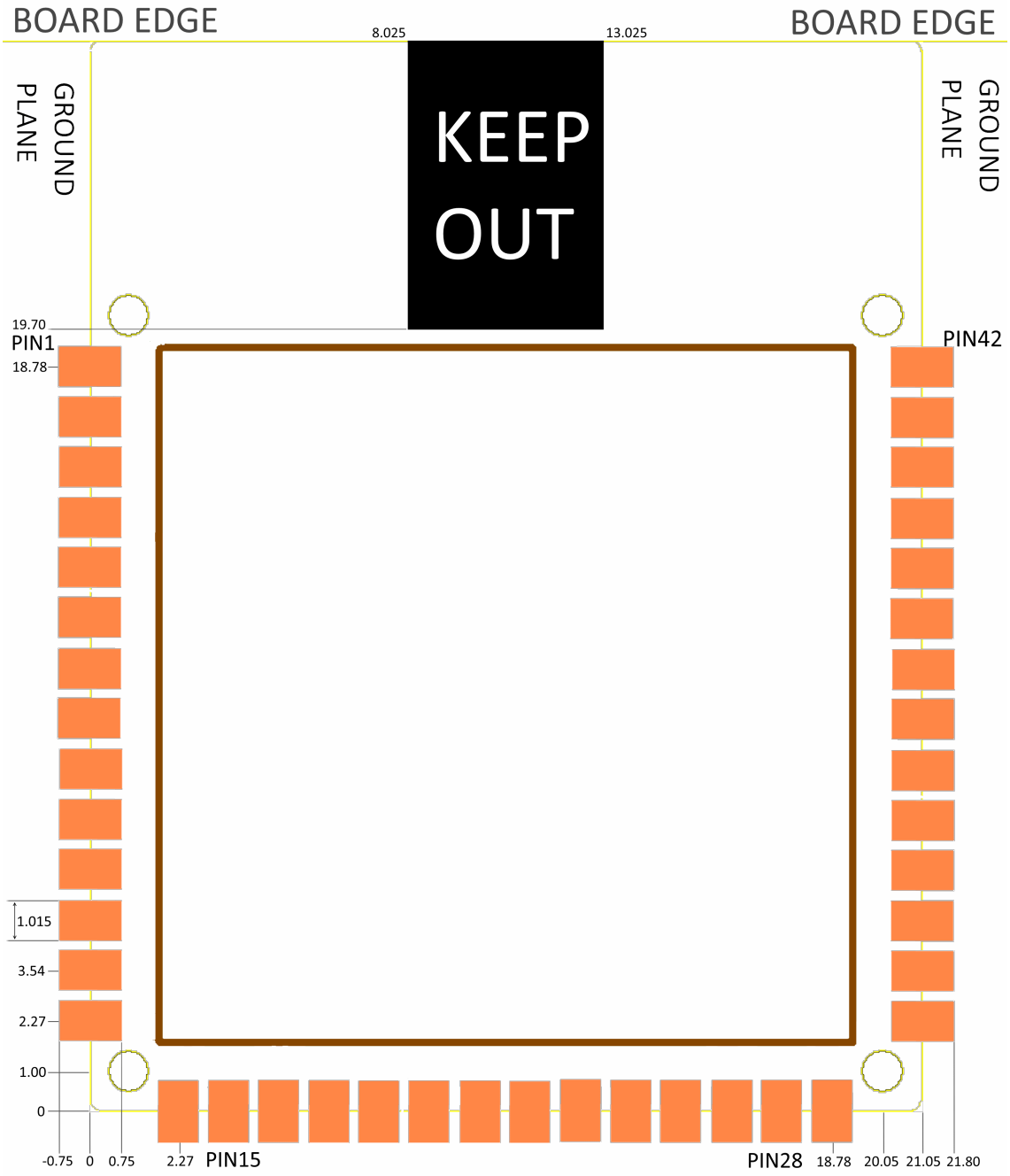

Figure 2.2: Chili2S Module Recommended Footprint (Unit:mm)

2.3 Pin Descriptions

Pin	Name	Type	M2351 Port	Description
1	VDD33	Supply	-	3.3V Power Supply
2	TMS	GPIO	PF.0	ICE/JLINK Data
3	GND	Ground	-	Module Ground
4	TCK	GPIO	PF.1	ICE/JLINK Clock
5	PB.12	GPIO	PB.12	General Purpose Digital I/O
6	PB.13	GPIO	PB.13	General Purpose Digital I/O
7	-	GPIO	PB.14	NC[1)]
8	-	GPIO	PC.1	NC[1)]
9	-	GPIO	PC.0	NC[1)]
10	TRSTX[3)]	Digital In	-	System Reset and ICE/JLINK Reset (active low)
11	PA.13	GPIO	PA.13	General Purpose Digital I/O
12	PA.14	GPIO	PA.14	General Purpose Digital I/O
13	VDD33	Supply	-	3.3V Power Supply
14	GND	Ground	-	Module Ground
15	PA.15	GPIO	PA.15	General Purpose Digital I/O
16	GND	Ground	-	Module Ground
17	PA.12	GPIO	PA.12	General Purpose Digital I/O
18	GND	Ground	-	Module Ground
19	GND	Ground	-	Module Ground
20	GND	Ground	-	Module Ground
21	GND	Ground	-	Module Ground
22	GND	Ground	-	Module Ground
23	GND	Ground	-	Module Ground
24	GND	Ground	-	Module Ground
25	GND	Ground	-	Module Ground
26	AVDD33	Supply	-	Filtered 3.3V Supply[2)]
27	GND	Ground	-	Module Ground
28	VDD33	Supply	-	3.3V Power Supply
29	-	-	-	NC[1)]
30	GND	Ground	-	Module Ground
31	PB.5	GPIO	PB.5	General Purpose Digital I/O
32	PB.4	GPIO	PB.4	General Purpose Digital I/O
33	PB.3	GPIO	PB.3	General Purpose Digital I/O
34	PB.2	GPIO	PB.2	General Purpose Digital I/O
35	PB.1	GPIO	PB.1	General Purpose Digital I/O
36	PB.0	GPIO	PB.0	General Purpose Digital I/O
37	-	GPIO	PF.5	NC[1)]
38	-	GPIO	PF.4	NC[1)]
39	-	GPIO	PA.3	NC[1)]
40	-	GPIO	PA.0	NC[1)]
41	-	GPIO	PA.2	NC[1)]
42	-	GPIO	PA.1	NC[1)]

Table 2.1: Chili2S Module Pin Descriptions

Notes:

1) NC: Do not connect, as pin is internally connected on module.
2) AVDD33 is a filtered supply output generated by the module for noise-sensitive peripherals. Do not connect to VDD33.
3) TRSTX (Pin 10) can be used by an external host to reset the Chili2S module. Leave unconnected if not used.

2.4 Multi-Function Pin (MFP) Mapping

The GPIO pins on the module can be assigned to specific functions including analog interfaces, communications interfaces and digital functionality. The table below summarises the MFP functions for all GPIO pins accessible on the module. For further information refer to the Nuvoton M2351 Technical Reference Manual [4].

Pin	GPIO Port	Default Function	Analog			Communications Interface					Digital					
			ADC	DAC	COMP	UART	I2C	SPI	USB	CAN	I2S	Smart Card	SD Card	PWM	QEI	Timer
2	PF.0	ICE TMS	-	-	-	UART1 TXD	I2C1 SCL	-	-	-	-	-	-	BPWM1 CH0	-	-
4	PF.1	ICE TCK	-	-	-	UART1 RXD	I2C1 SDA	-	-	-	-	-	-	BPWM1 CH1	-	-
5	PB.12	UART0 RXD	EADC0 CH12	DAC0 OUT	ACMP0 P2[3]	UART0 RXD	I2C2 SDA	-	-	-	-	-	SD0 nCD	EPWM1 CH3	-	TM3 EXT
6	PB.13	UART0 TXD	EADC0 CH13	DAC1 OUT	ACMP0 P3[4]	UART0 TXD	I2C2 SCL	-	-	-	-	-	-	EPWM1 CH2	-	TM2 EXT
11	PA.13	GPIO PA.13	-	-	-	UART4 RXD	I2C1 SDA	SPI2 CLK	D-	CAN0 RXD	I2S0 MCLK	SC2 RST	-	BPWM1 CH3	QEI1 A	-
12	PA.14	GPIO PA.14	-	-	-	UART0 TXD	I2C2 SCL	SPI2 MISO	D+	-	I2S0 DI	SC2 DAT	-	BPWM1 CH4	QEI1 B	-
15	PA.15	GPIO PA.15	-	-	-	UART0 RXD	I2C2 SDA	SPI2 MOSI	OTG ID	-	I2S0 DO	SC2 CLK	-	BPWM1 CH5[5]	-	-
17	PA.12	GPIO PA.12	-	-	-	UART4 TXD	I2C1 SCL	SPI2 SS	VBUS[8]	CAN0 TXD	I2S0 BCLK	SC2 PWR	-	BPWM1 CH2	QEI1 INDEX	-
31	PB.5	GPIO PB.5	EADC0 CH5	-	ACMP1 N	UART5 TXD	I2C0 SCL	SPI1 MISO	-	-	I2S0 BCLK	SC0 CLK	SD0 DAT3	EPWM0 CH0	-	TM0
32	PB.4	GPIO PB.4	EADC0 CH4	-	ACMP1 P1	UART5 RXD	I2C0 SDA	SPI1 MOSI	-	-	I2S0 MCLK	SC0 DAT	SD0 DAT2	EPWM0 CH1	-	TM1
33	PB.3	GPIO PB.3	EADC0 CH3	-	ACMP0 N	UART1 TXD[1]	-	SPI1 CLK	-	-	I2S0 DI	SC0 RST	SD0 DAT1	EPWM0 CH2	-	TM2
34	PB.2	GPIO PB.2	EADC0 CH2	-	ACMP0 P1	UART1 RXD[2]	-	SPI1 SS	-	-	I2S0 DO	SC0 PWR	SD0 DAT0	EPWM0 CH3	-	TM3
35	PB.1	GPIO PB.1	EADC0 CH1	-	-	UART2 TXD	I2C1 SCL	-	-	-	I2S0 LRCK	-	SD0 CLK	EPWM0 CH4[6]	-	-
36	PB.0	GPIO PB.0	EADC0 CH0	-	-	UART2 RXD	I2C1 SDA	-	-	-	-	-	SD0 CMD	EPWM0 CH5[7]	-	-

Table 2.2: Multi-Function Pin (MFP) Functionality for the Chili2S GPIO Pins

Notes:

1) Also programmable as UART5_nRTS
2) Also programmable as UART5_nCTS
3) Also programmable as ACMP1_P2
4) Also programmable as ACMP1_P3
5) Also programmable as EPWM_SYNC_IN
6) Also programmable as EPWM1_CH4 or EPWM0_BRAKE0
7) Also programmable as EPWM1_CH5 or EPWM0_BRAKE1
8) If pin 17 (PA.12) is used as USB VBUS, note that this is a standard 3.3V I/O pin and should **not** be connected to 5V. Two diodes should be connected in series for a 1.5V voltage drop to safely connect VBUS from a USB host to pin 17.

2.5 JTAG/SWD ICE Connector for Programming and Debug

A footprint is supplied on the bottom side of the module for a 10-pin connector to directly connect a programmer or debugging interface, for example a Segger J-Link Debug Probe.

TRSTX	10	9	GND
NC	8	7	GND
NC	6	5	GND
TCK	4	3	GND
TMS	2	1	VDD33

Figure 2.3: 10-Pin Header for JTAG/ICE Programming and Debug

Note that the Pinout in Figure 2.3 shows the module bottom side view and is therefore mirrored compared to the footprint indication on the top left of Figure 2.1.

Note that all JTAG/SWD signals can also be accessed via the edge pads of the module.

2.6 Power Supply

All VDD33 pins (pins 1, 13 and 28) are connected to the same net on the module, therefore only one connection is required to supply the module. It is however recommended to connect as many as VDD33 pins as possible to decrease impedance for the power connections. No additional external components such as supply filters are required.

AVDD33 is a filtered version of VDD33 used both on the module and connected to pin 26 as analog power output, so it can be used to supply noise-sensitive off-module peripherals. It should **not** be connected to VDD33.

2.7 RF Circuitry

The Chili2S module uses a passive balun design for impedance matching and converting the differential signal of the CA-8211 to a single-ended 50Ω signal for connecting the SMD chip antenna.

When mounting the Chili2S module onto a host board, the module top edge should be aligned with the board edge with the antenna facing out, see Figure 2.2. To maximise range, an adequate ground plane must be provided on the host PCB. Correctly positioned, the ground plane on the host PCB will contribute significantly to the antenna performance. The area around and under the antenna, marked KEEP OUT, must be kept clear of conductors or other metal objects on any layer of the host board.

3 Electrical Specification

This section specifies important parameters for the Chili2S module. For more detailed information refer to the Nuvoton M2351 Datasheet [3] and the Cascoda CA-8211 Datasheet [2].

3.1 Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Voltage (on any pin)		-0.3	-	3.9	V
Storage Temperature Range		-65	-	150	°C
Input RF Level		-	-	+10	dBm

Table 3.1: Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the module. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Environmental Conditions

Parameter	Conditions	Min	Typ	Max	Units
ESD	Human-body model, JEDEC STD 22	-	-	2000	V
	Charged-device model, JEDEC STD 22	-	-	500	V
MSL		MSL3			

Table 3.2: Environmental Conditions

3.3 Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Supply Voltage – Device Supply (VDD33)	2.1	-	3.6	V
Operating Temperature	-40	-	85	°C

Table 3.3: Recommended Operating Conditions

3.4 Digital Pin Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Low Voltage (TTL Input)	V_{IL}	VDD33=3.3V	-	-	0.8	V
Input High Voltage (TTL Input)	V_{IH}	VDD33=3.3V	2.0	-	-	V
Pull-up Resistor	R_{PU}		-	53	-	kΩ
Input Leakage Current @ V_I=3.3V	I_I		-	-	1	uA
Output Sink Current	I_{OL}	VDD33=3.3V, Vin=VSS+0.4V	3.6	-	19.9	mA
Output Source Current	I_{OH}	VDD33=3.3V, Vin=VDD33-0.4V	-20.6	-	-3.4	mA

Table 3.4: Digital Pin Characteristics

3.5 Supply Currents

Specified for VDD33=3.3V, T=25'C, System Clock=16MHz.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Transmit	$I_{DD_{Tx}}$	Tx Power +9 dBm Tx Power 0 dBm		20 13		mA mA
Receive	$I_{DD_{Rx}}$	-105 dBm Sensitivity		15		mA
Processor active, Radio Off	$I_{DD_{ACTIVE}}$			1.5		mA
Sleep Mode	$I_{DD_{SLEEP}}$			3		uA

Table 3.5: Supply Currents

3.6 General RF Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency Range	I_{FR}	As specified by [1]	2405		2480	MHz
Number of Channels		As specified by [1]		16		
Data Rate	DR	As specified by [1]		250		kbit/s
TX/RX Turnaround Time		As specified by [1]			192	µs

Table 3.6: General RF Characteristics

3.7 Receiver RF Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Receiver Sensitivity		1% PER, PSDU 20 bytes		-105		dBm
Maximum Receiver Input Level		1% PER, PSDU 20 bytes		0		dBm
Symbol Rate Tolerance			-80		80	ppm
Adjacent Channel Rejection Low		-5 MHz		22		dB
Adjacent Channel Rejection High		+5 MHz		35		dB
Alternate Channel Rejection Low		-10 MHz		50		dB
Alternate Channel Rejection High		+10 MHz		50		dB
Spurious Emissions		30 MHz – 1 GHz 1 GHz – 12.75 GHz		-77 -52		dBm dBm
ED Range				83		dB
ED Low Range Limit				-104		dBm
ED High Range Limit				-21		dBm
ED Accuracy within Range				±2		dB
ED LSB Value				0.5		dB

Table 3.7: Receiver RF Characteristics

3.8 Transmitter RF Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Power			0		9	dBm
Transmitter EVM				5	10	%
Transmitter Harmonics 2nd Harmonic 3rd Harmonic		@9dBm transmit power		 -52 -74		dBm
Transmitter Spurious Emissions		30 – ≤1000MHz >1 – 12.75GHz 1.8 – 1.9GHz 5.15 – 5.3GHz		-77 -50 -68 -67		dBm
Absolute PSD Limit		|F-Fc|>3.5MHz		-43		dBm
Relative PSD Limit		|F-Fc|>3.5MHz		-35		dB

Table 3.8: Transmitter RF Characteristics

4 Software Support

The Cascoda open-source Software Development Kit (SDK) is available on GitHub (https://github.com/Cascoda/cascoda-sdk) and contains the API, drivers and interfaces required for developing applications using OpenThread or custom IEEE 802-15-4 based network connectivity.

The Cascoda SDK kit for the Chili2S module and the Nuvoton M2351 MCU contains:

- Optimised and exhaustively tested MAC-level (MCPS/MLME) API and interface drivers
- Hardware-MAC interface and configuration for OpenThread, an open-source implementation of the Thread® IPv6 based wireless mesh networking stack (https://openthread.io/)
- Example library for sensor interface drivers
- Low power modes
- Examples for custom IEEE 802.15.4 MAC based applications
- Hardware abstraction functions for module I/O handling , timers etc.

Build Environment

The Cascoda SDK makes full use of CMake as a build system, to enable advanced configuration and cross-platform development in combination with the ARM® GCC compiler toolchain. Build environments for other embedded compilers (IAR, Keil) are also available.

5 Regulatory Approvals

EC, FCC and ISED certification and modular approval is in progress.

6 Soldering Information

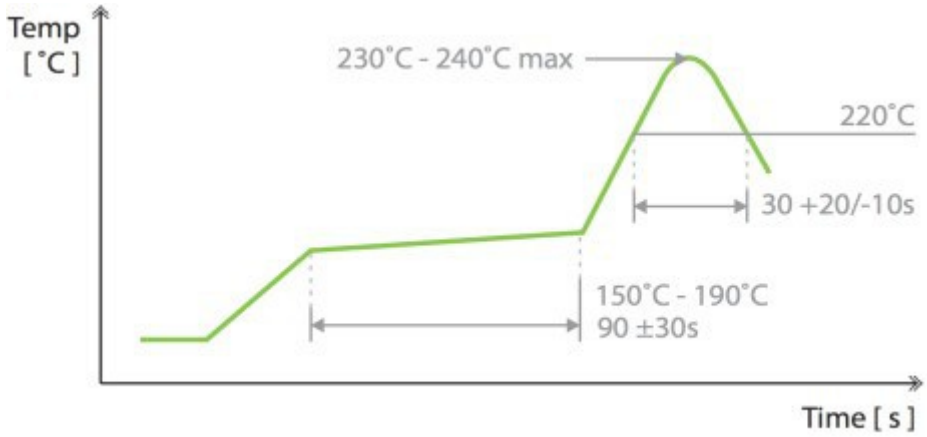

Figure 6.1: Soldering Temperature Time Profile for Reflow Soldering (Lead−Free Solder)

Cycles: it is recommended to do only one soldering cycle.

Cleaning: it's not recommended to clean the module. Solder paste residuals underneath the module cannot be removed.

7 References

[1] IEEE Std 802.15.4™-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)

[2] Cascoda IEEE 802.15.4 Transceiver CA-8211 Datasheet, Rev. 1.0, January 2019, https://www.cascoda.com/wp-content/uploads/2019/01/CA-8211_datasheet_0119.pdf

[3] Nuvoton NuMicro® Family M2351 Series Datasheet, Rev. 1.01, Feb 15, 2019, http://www.nuvoton.com/resource-files/DS_M2351_Series_EN_Rev1.01.pdf

[4] Nuvoton NuMicro® Family M2351 Series Technical Reference Manual, Rev. 1.00, Aug, 2018, http://www.nuvoton.com/resource-files/TRM_M2351_Series_EN_Rev1.00.pdf

8 Revision History

Revision	Date	Status	Comments
0.1	07 May 2019		Pre-Release, for Review only.
0.2	30 May 2019		Update image on the first page
0.3	05 July 2019		Update Image on the first page
0.4	26 July 2019		Update Chili2S Block Diagram
0.5	03 Sep 2019		Preliminary Release