Application Note

PCB Design Considerations for the CA-8210

Release, Rev. 1.0, January 2018

Revision Control

Date	Contributors	Revision	Comments
12/01/18	B. Johnson	1.0	Created

Application Note

PCB Design Considerations for the CA-8210

Release, Rev. 1.0, January 2018

Table of Contents

1 Introduction

This application note is intended to be used by design engineers to ensure that the design and layout of the CA-8210 2.4 GHz IEEE® 802.15.4 transceiver modem conforms to specification.

The example given in this application note is for a module that connects to general purpose microcomputer boards through a UEXT connector. However, the design and layout considerations are applicable to any layout of the CA-8210.

No antenna has been included in this application note. The reason for this is that antenna layout any matching is highly dependent on a number of factors that are out of the scope of this application note. Cascoda will issue separate antenna application notes in due course.

2 General

The CA-8210 device has four distinct domains. These domains are the radio frequency (RF), the PLL, the analog and the digital domains.

The illustration below shows how these four domains should surround the device.

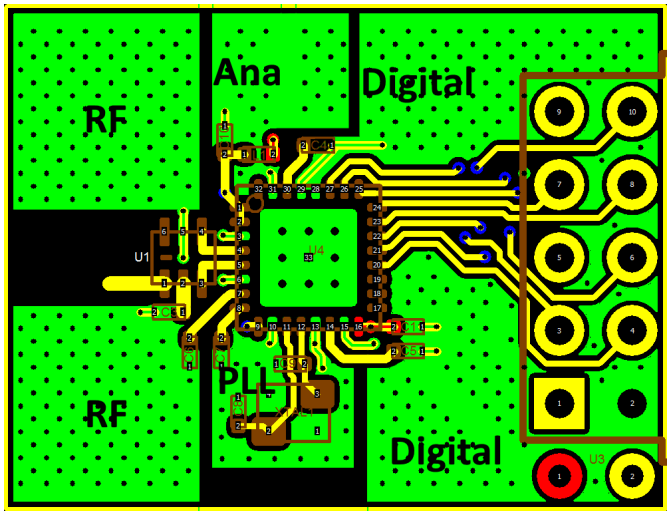


Illustration 1: PCB top layer

Each domain should be separated by 0.5mm, so as to minimize noise coupling between domains.

No connections are made between the CA-8210 ground pad and any of the ground pins at the top level of the PCB.

3 Ground

To ensure a low impedance ground connection from the ground pad of the CA-8210 through to the bottom of the PCB, the footprint land pattern used for the QFN32 device should have nine plated vias, each with a drill dimension of 0.3-0.33mm. In addition, it is essential that ground vias are placed as close as possible to all ground pins.

3.1 Star ground philosophy

A star ground philosophy should be used, which defines a single ground point to which all voltages from all domains are referred. The star ground point for the layout is the point at which the vias of the of the QFN32 ground pad bisect the domain ground layers.

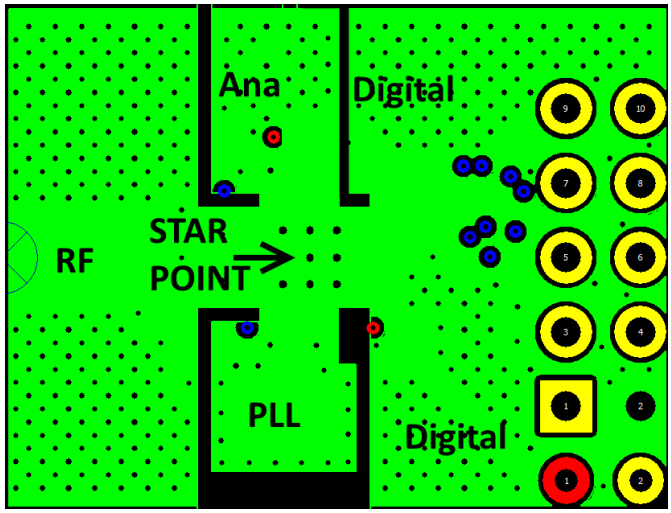


Illustration 2: PCB top layer - 1

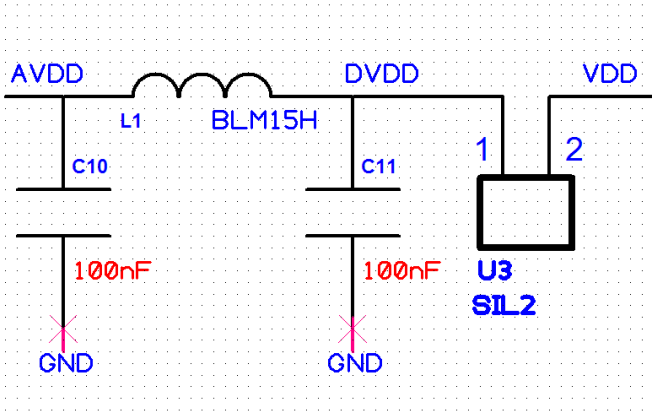
As with the top level of the PCB, each ground domain should be separated by 0.5mm, so as to minimize noise coupling between domains.

4 Power Supply

The supply to the CA-8210 must be divided into two domains as follows:

- DVDD: Supply to the Digital regulators
- AVDD: Supply to the Analog peripherals and regulators

The following filter circuit should be used to ensure that the supply to the analog regulators is sufficiently clean. Jumper SIL2 is optional.



Note that the ground used for C10 (AVDD) should refer to the Analog ground domain, while the ground used for C11 (DVDD) should should refer to the Digital ground domain.

5 RF considerations

The CA-8210 device has been carefully designed to present a balanced impedance of 100Ω at the differential RF input/output pins, RFP and RFN.

In order to match the balanced and unbalanced impedance tracks on a PCB, the tracks should be treated as microstrip transmission lines. As such, a set of equations must be used to calculate the characteristic impedance of the microstrip. These equations take as their input the relative permittivity of the PCB substrate material, the width of the strip, the thickness of the substrate and the frequency of interest.

There are many online tools that facilitate the design of such microstrips, both balanced and unbalanced.

Note that the choice of the PCB layer used for the RF ground is best determined by the matching requirement of the balanced microstrip, see below.

5.1 Connecting the CA-8210 to a balun

The differential RF pins, RFP and RFN must be connected to a balanced microstrip, impedance matched to 100Ω.

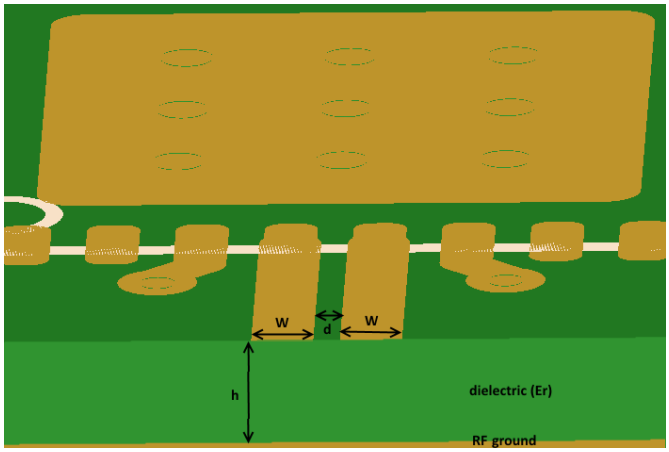


Illustration 3: 100Ω balanced microstrip

5.2 Connecting the balun to an antenna

The single ended RF pin from the balun must be connected to a microstrip impedance matched to 50Ω.

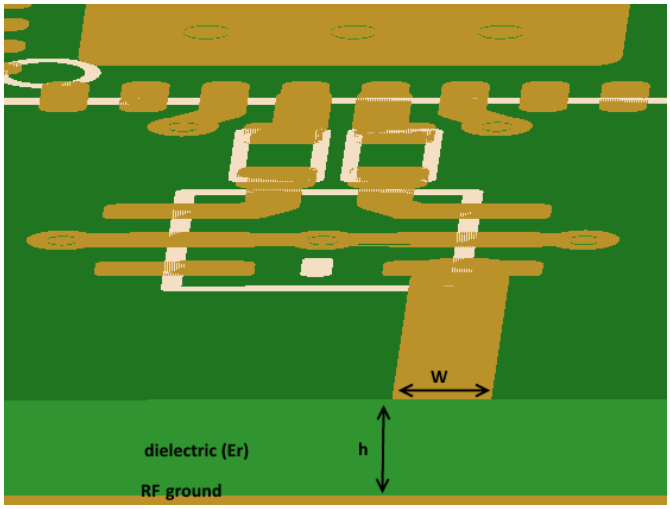


Illustration 4: 50Ω unbalanced microstrip

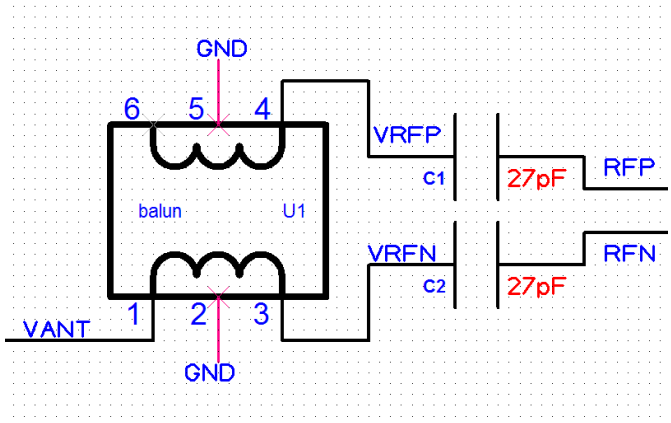
5.3 Balun connection

Baluns can be connected directly to the differential RF input/output of the CA-8210 device, or via coupling capacitors.

5.3.1 Coupled balun configuration

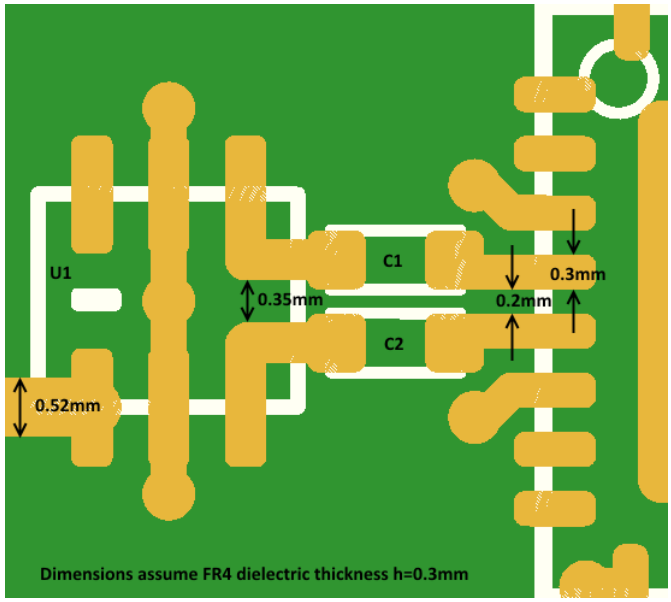
The advantage of using coupling is that the coupling capacitor value can be used to adjust for small impedance mismatches between the CA-8210 device and the balun. The disadvantage of this configuration is that it takes up more space on the PCB.

The schematic of the coupled balun configuration is given below:



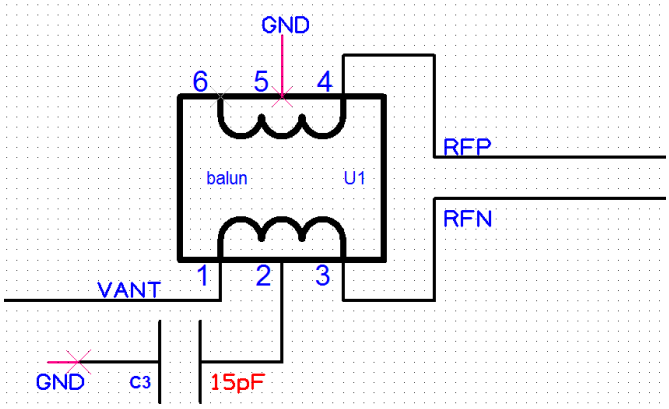
Note that in this configuration pin 2 of the balun is grounded, while pin 6 is not connected.

The recommended layout for the coupled balun connection is given below:



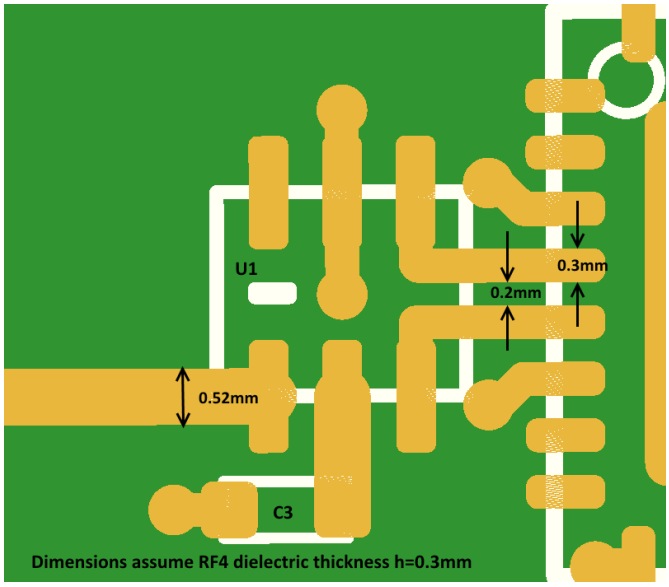
5.3.2 Direct balun configuration

The direct balun configuration requires careful layout and unlike the coupled configuration cannot be tuned after manufacture. However, it does result in a more compact layout. The schematic of the direct balun configuration is given below:



Note that in this configuration pin 2 of the balun is connected to a RF capacitor that maintains the correct common-mode bias point, while pin 6 is not connected.

The recommended layout for the direct balun connection is given below:



The dimensions given in the layout above assume that the RF ground layer is a solid sheet of metal 0.3mm below the top layer shown.

5.4 Copper pour

Most PCB design tools have a copper pour function. Copper pour should not be used close to a microstrip transmission line since the RF ground should be the dominant ground reference. Instead, RF ground vias and ground connections should be made manually.

6 PLL and crystal considerations

The crystal oscillator shares the same ground domain as the PLL. The CA-8210 device has two ground pins for this domain, namely pin 10 & 13. These pins are either side of the crystal pins. A via should be placed as close as possible to these ground pins.

A copper pour area should be defined around the crystal and the associated padding capacitors, C8 and C9. This area should be connected to the PLL ground domain using plenty of vias. Lastly, the regulator decoupling capacitor C7, for AVDD1, should use the PLL ground domain.

The resulting layout is illustrated below:

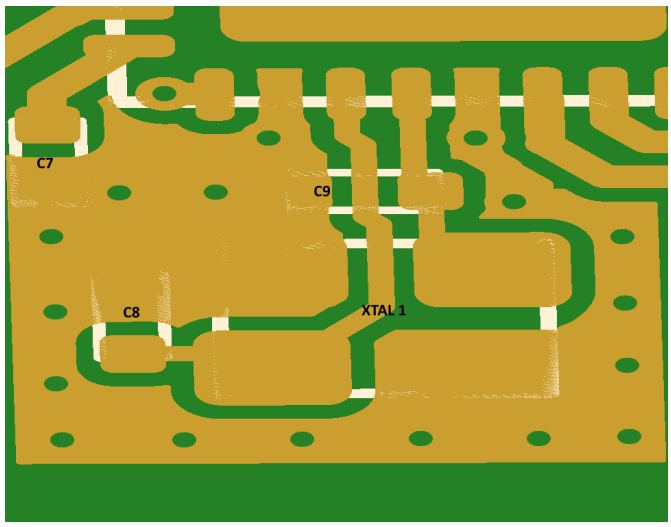


Illustration 5: Crystal layout & PLL domain

7 External clock considerations

The CA-8210 will accept an external 16MHz clock source. In this configuration, pin XTA16MQ2 should be connected to the PLL domain ground. The clock should be applied to pin XTA16MQ1, with an amplitude between 1.0V to 1.8V.

If an external clock is required, the phase noise and accuracy of this clock must be within the tolerances determined by the IEEE® 802.15.4 specification.

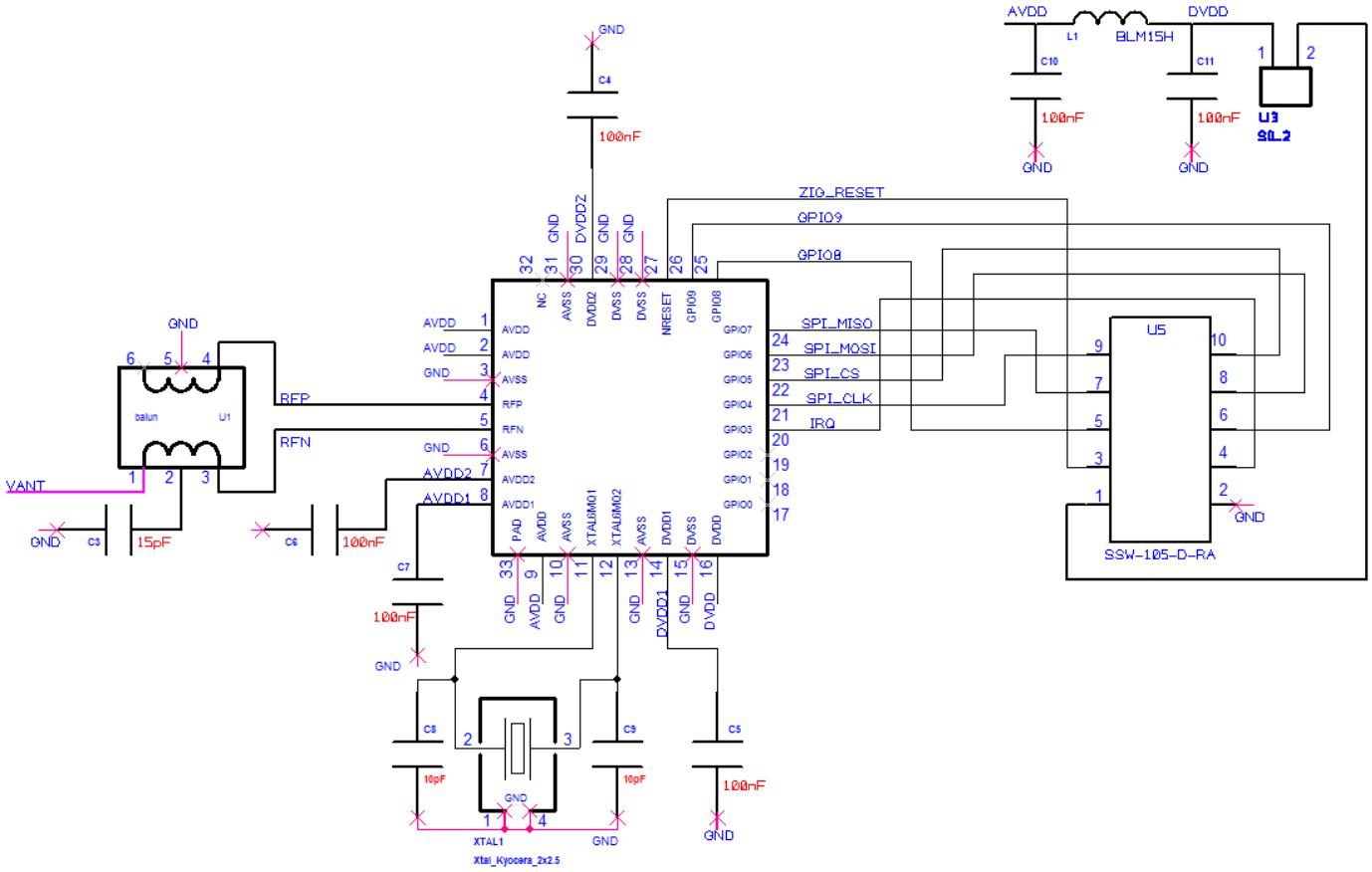
The spectral purity of this clock means that care must be taken to minimise spurious emissions. As such a first order RC filter should be used. This RC filter should be referred to the PLL domain ground.

Please contact Cascoda for further details.

8 Clock output driver

As with using an external clock, should the internal clock output be enabled, the spectral purity of the clock from the CA-8210 means that a first order RC filter should be used to minimise spurious emissions. In this case, Cascoda recommends a first order filter with a 3dB cut-off frequency of 100MHz.

9 Schematic



10 Recommended components

Cascoda recommends the following components:

Component	Size	Ground domain	Value	Part Number
balun U1[1]	0805	RF	50Ω/100Ω (Unbalanced/ balanced)	Wurth: 748421245 Johanson: 2450BL15B100
RF capacitor, C1, C2	0402	RF	27pF	201R07S270JV4S
RF capacitor, C3	0402	RF	15pF	201R07S150JV4S
C4, C5	0402	Analog	100nF	any
C6	0402	RF	100nF	any
C7	0402	RF	100nF	any
C10	0402	Analog	100nF	any
C11	0402	Digital	100nF	any
L1	0402	Digital->Analog	<2Ω	Murata BLM15H series
C8, C9	0402	PLL	10pF	any
Crystal	2.5mm x 2mm	PLL	16.0000 MHz	AVX/Kyocera: CX252016000D0FZZC1 Epson: FA-20H 16.0000MF10Z

Table 1: Recommended components

1 More baluns will be added in time.

Cascoda Ltd
1 Venture Road
Southampton Science Park
Southampton, SO16 7NP
United Kingdom
Tel.: +44 (0)2380 111797
Email: info@cascoda.com